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REMARKS

The above-noted amendments are presented in response to the Office Action of November 7, 2003 , wherefore reconsideration is requested.

Referring now to the text of the Office Action:

a) claims 32, 35, 36 and 38-38-66 stand objected to because of informalities noted by the Examiner in claim 32;

b) claims 67 and 68 stand rejected under 35 U.S.C. § 102(b), as being unpatentable over the teaching of United States Patent No. 5,512,860 (Huscroft et al.);

c) claims 1-32, 35, 36 and 38-38-66 are allowable over the prior art, subject to correction of the above-noted deficiencies in claim 32; and

d) claims 69-78 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims.

As an initial matter, applicant appreciates the Examiner's indication of allowable subject matter in claims 1-32, 35, 36, 38-38-66 and 69-78. It is believed that the Examiner's objections to claims 32, 35, 36 and 38-66, and rejected claims 67 and 68 are overcome by the above-noted claim amendments, and further in view of the comments below.

In support of his rejection of claims 67 and 68, the Examiner asserts that Huscroft et al discloses "... sampling (FIG. 1) the received data signal using a phase detector (FIG. 1, block 5) that generates a phase error signal indicative of a detected phase difference between the data signal and an oscillator output signal and an digital frequency detector (FIG. 1, 15)". Applicant disagrees.

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United States Patent No. 5,512,860 (Huscroft et al.) teaches a clock recovery circuit for recovering a clock signal from an input data signal (RSD). As shown in FIG. 1, and described at Col. 4, lines 24-33, the input data signal is supplied to the phase detector 5. Thus:

> The basic phase locked loop is comprised of a voltage controlled oscillator (VCO) 1, the output of which is applied to the input of a mode divider 3, the output of which is connected to the input of a phase detector 5, the output of which is connected to the input of the VCO through a loop filter 7. The output of the phase detector is connected to the loop filter through a multiplexer, to be described in more detail below. An input data signal RSD (referred to below as the input data signal) from which the clock is to be recovered is applied to another input of phase detector 5.

On the other hand:

> "A reference phase/frequency detector 15 receives at one input the DCLK output signal of the reference divider 13 and at another input a reference clock signal REFCLK. This detector compares the signals at its inputs, and generates up or down pulses that are fed to the loop filter in place of the pulses output from phase detector 5. These should always drive the VCO to a true lock condition to the reference clock REFCLK, regardless of the operating frequency of the VCO. This detector 15 should be a true phase/frequency detector." (Col 5, lines 31-39)

Accordingly, and contrary to the Examiner's characterization, it will be clear that only the phase detector 5 samples the input data signal. The frequency detector 15 samples the "DCLK output signal of the reference divider 13 and ... a reference clock signal REFCLK", and does not receive the input data signal (see also FIG. 1).

In direct contrast, claim 67 includes a step of " sampling the received data signal using a phase detector ... and a digital frequency detector ...". Thus claim 67 clearly defines that the data signal is sampled by both the phase and frequency detectors. Huscroft et al. does not teach that the input data signal is sampled by both the phase and

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frequency detectors, as defined in the present invention Thus it is believed that independent claim 67, and its dependencies are clearly distinguishable over the teaching of Huscroft et al.

In light of the foregoing, it is believed that the present application is in condition for allowance, and early action in that respect is courteously solicited.

If any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this response, such extension is hereby respectfully requested. If there are any fees due under 37 C.F.R. §§ 1.16 or 1.17 which are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 19-5113.

Respectfully submitted,

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